REMARKS/ARGUMENTS

The foregoing proposed amendment presents amended claims 1, 2, 3, 8 and 11, original claims 4-7, 9-10, and 12-13 and added claims 14-15. As a result of this amendment, claims 1-15 remain in the application. Allowance of claims 1-15 as amended is respectfully requested.

The examiner objected to the drawings for failing to show a discriminator in a feedback loop and a phasor. Previous FIGs. 4 and 4a illustrated a phasor. Prior FIG. 3 illustrated an AGD calculator 310 that is part of the feedback loop back to the demodulator 301. As described in paragraph 0033, the discriminator can be part of the feedback loop and can be contained within the AGD calculator 310. FIG. 3 and the specification has been amended to include a block diagram illustrating where the discriminator can reside as item 311. Although the prior diagram showed every feature of the invention within a block diagram as described in the specification, the replacement sheet now includes an explicit reference to the discriminator. Thus, every feature claimed is shown in the drawings and no new matter is included by this amendment.

The Examiner rejected claim 2, 6-7 and 10 under 35 USC section 112, first paragraph for failing to comply with the enablement requirement.

With respect to claim 2, a discriminator in a feedback loop has been described in the specification in paragraph 0033 such that the timing offset can be directly determined from the OFDM symbols using a discriminator feedback loop. Furthermore, it should be noted that discriminators in feedback loops are known in other systems such as in Intersil's HSP50110 Digital Quadrature Tuner that includes the Digital Costas Loop (DCL) that performs many of the baseband processing tasks required for the demodulation of BPSK, QPSK, 8-PSK, OQPSK, FSK, AM and FM waveforms such as carrier phase error detection or tracking and symbol synchronization (See block diagrams on pages 3-1 and 3-4.) One of ordinary skill in the art can easily implement a discriminator in the feedback loop of FIG. 3 of Applicant's embodiment.

With respect to claim 6, the rationale for such embodiments is addressed in the background where current symbol timing recovery for XM digital audio radio is based on Amplitude Modulated Synchronization Symbol (AMSS) that can become highly corrupted with high delay spreads and/or when a vehicle is stopping or is stopped. In certain conditions, with no

AMSS detected, the Multicarrier Modulation (MCM) demodulator can drift out of lock. In another instance, the channel can have delayed signal(s) that are stronger than the earlier arriving signal. The current AMSS algorithm tends to lock onto the strongest signal rather than the desired earliest signal, causing severe intersymbol interference. Thus, the method and apparatus claimed can provide reliable symbol timing in conditions where current OFDM symbol synchronization is susceptible to corruption or intersymbol interference.

Further, referring to paragraph 0040 and FIG. 6, the specification and flow chart clearly discusses narrowing a search window for a synchronization symbol and adjusting the timing to an earlier arriving signal detected by a synchronization symbol recovery detector after detecting a negative phase in an OFDM modulated signal at decision block 602. Narrowing a search window for a synchronization window and adjusting timing should be well known to one ordinarily skilled in the art as exemplified by the narrowing window used in the IS-95 specification for CDMA cellular communications and the adjusted timing used for indoor communications for multi-user detection (MUD) algorithms as described in a paper by Paul James Husted.

Likewise, with respect to Claim 7, disabling a synchronization symbol recovery algorithm is clearly taught in FIG. 7 and in paragraph 0040. Disabling a synchronization symbol recovery algorithm should be self explanatory. If a negative timing offset from the AGD calculator (310) is detected, then a synchronization symbol recovery algorithm is disabled. The timing can be adjusted until a non-negative phase is detected. In other words, at step 706,